# coreboot on RISC-V — 2018 Edition

Jonathan Neuschäfer

OSFC 2018

# About myself

- Jonathan Neuschäfer
- student
- worked on coreboot/RISC-V during GSoC 2016 (with Ron Minnich)
- became the maintainer for coreboot/RISC-V

# Why coreboot?

- interested in hardware initialization
  - the “lower half” of firmware
- coreboot provides a unified “lower half”
- different “upper halves” through payloads
  - u-boot, Depthcharge, LinuxBoot, UEFI, bbl, ...
- active community

# New hardware: SiFive FU540

- "HiFive Unleashed" devboard released in spring
- RV64IMAFDC x4
- RV64IMAC x1
- 8GiB DDR4 RAM with ECC
- Gigabit Ethernet
- SPI/I²C/GPIO/UART/...
- ChipLink extension interface

# New contributors

- Xiang Wang and Shawn C. from HardenedLinux
- Philipp Hug
- long time members of the coreboot community helped review some code

# SiFive FU540 port history

- started in April with UART driver and `soc` directory
- asked SiFive to release DDR4 config data for H5U
  - at first they refused
  - later promised to open-source FSBL
  - https://github.com/sifive/freedom-u540-c000-bootloader/
- Xiang Wang and Philipp Hug started sending patches
- started to review these patches two weeks ago

# Unsolved problems

- ~~FU540 RAM init~~
- good SMP support
- Linux file format (physical vs. virtual addresses)
- support for more hardware and payloads
- security of M-mode code
- loading M-mode code from the payload/kernel

# Thank you for listening!

```
    la t0, answer
    csrw mtvec, t0

questions:
    wfi
    j questions
```